REMARKS

The above amendments and these remarks are responsive to the Office Action issued on May 5, 2004. By this response, claims 1, 5 and 9 are amended, and claims 2, 3, 6 and 7 are cancelled without prejudice. Claims 10-12 are newly presented. The title of the application also is amended. No new matter is added. Claims 1, 4, 5 and 8-12 are now active for examination.

The Office Action dated May 5, 2004 rejected claims 1-9 under 35 U.S.C. §102(b) as being anticipated by Poisner (U.S. Patent No. 6,012,154). The Examiner objected to the title of the application for being non-description. It is respectfully submitted that the claim rejection is traversed and the objection is addressed, in view of the amendments and remarks presented herein.

The Anticipation Rejection of Claims 2, 3, 6 and 7 Is Now Moot

By this Response, claims 2, 3, 6 and 7 are cancelled without prejudice. Accordingly, the anticipation rejection of claims 2, 3, 6 and 7 is now moot.

The Anticipation Rejection Is Traversed

Claims 1, 4, 5, 8 and 9 were rejected as being anticipated by Poisner. By this Response, claims 1, 5 and 9 are amended. The anticipation rejection is respectfully traversed because Poisner cannot support a prima facie case of anticipation.

Claim 1, as amended, is directed to a method of supervising a failure of a system using a plurality of timers, such as watch dog timers (WDT), for gradually recovering from system failures using different recovery approaches. A selected one of the timers is

activated and determined whether it has been reset or not (step (a)). If the timer has not been reset, the timer starts to count down (step (b)). If the timer is timed out after a predetermined period of time, a signal for recovery from the failure is generated and a corresponding one of the steps of (i) setting a flag, (ii) outputting an interrupt signal, (iii) outputting a non-maskable interrupt and (iv) outputting a system reset signal, is performed (steps (c) and (d)). If the failure cannot be recovered, then steps (a) to (d) are repeated for another one of the plurality of timers (step (e)). Each time when the signal for recovery is generated, a corresponding one of steps (i) to (iv) is executed in a manner that steps (i) to (iv) are executed sequentially one by one when steps (a) to (e) are repeatedly executed. This sequencing of the steps (i) to (iv) progressively recovers the system from the failure in accordance with the degree of the failure.

Furthermore, a plurality of conditions are provided for resetting the timers. The plurality of conditions corresponds to sets of values set in a plurality of registers. The plurality of reset conditions allows monitoring of more than one device or operating system. For instance, each processor in a multi-processor environment is configured to reset an assigned register from time to time. If any of the registers is not properly reset, it indicates that one of the processors is not working properly, and steps (a) to (e) are performed as described earlier. Appropriate support for the amendment can be found in, for example, Figs. 1-4; page 3, line 23 though page 4, line 19; and page 10, line 2 through page 11 line 5.

Unlike the method of claim 1 that uses a plurality of timers, Poisner only discusses executing a plurality of proceedings, such as interruption, reactivation, etc., in a stepwise manner by using the same timer. For example, Poisner's system does not have the capacity to monitor operations of each of a plurality of processors. Poisner also fails to teach

providing a plurality of registers for storing values to be compared with a plurality of conditions, as described in claim 1. Moreover, Poisner does not disclose that if the failure cannot be recovered, then steps (a) to (d) are repeated for another one of the plurality of timers, as described in claim 1. Since Poisner fails to teach every limitation of claim 1, Poisner cannot support a prima facie case of anticipation. The anticipation rejection based on Poisner is untenable and should be withdrawn. Claim 4 depends on claim 1 and incorporates every limitation thereof, and further describes that the step executed in accordance with the signal generated in step (d) is recorded. This feature is not taught in Poisner. Thus, claim 4 is patentable over Poisner based on the same reasons for claim 1 as well as on its own merits. Favorable reconsideration of claims 1 and 4 is respectfully requested.

Independent claim 5 relates to an apparatus for supervising a failure of a system using a plurality of timers and a plurality of registers. The apparatus includes various means (a) to (e) for activating one of the plurality of timers and determining whether the activated timer is reset or not; for counting down the activated timer if not reset; for determining whether the activated timer has gone time out at a predetermined time; for generating a signal for recovery from the failure in the case where the activated timer has gone time out; and for executing a corresponding one of the steps of (i) setting a flag, (ii) outputting an interrupt signal, (iii) outputting a non-maskable interrupt and (iv) outputting a system reset signal, responsive to the signal for recovery being generated. A further means (f) is provided for activating means (a) to (e) for another one of the plurality of timers if the failure cannot be recovered after activating means (e). Each time the signal for recovery is generated, means (e) executes a corresponding one of steps (i) to (iv) in a manner that steps (i) and (iv)

are executed sequentially one by one when means (a) to (e) are repeatedly activated. Furthermore, a plurality of conditions are respectively set for resetting the plurality of timers. The plurality of conditions correspond to plural sets of values set in the plurality of registers. A reset operation to be executed on one of the plurality of registers corresponds to one of the plurality of conditions each time means (f) is activated. Appropriate support for the amendment can be found in, for example, Figs. 1-4; page 3, line 23 though page 4, line 19; and page 10, line 2 through page 11 line 5.

As discussed above, Poisner only uses one timer in the failure recovery process. Therefore, Poisner fails to teach using a plurality of timers to be activated sequentially to recover the system from failures, as described in claim 5. In addition, Poisner fails to disclose means (f) for activating means (a) to (e) for another one of the plurality of timers if the failure cannot be recovered after activating means (e), as described in claim 5. Moreover, Poisner also fails to teach providing a plurality of registers for storing values to be compared with a plurality of conditions, as described in claim 5. Since Poisner fails to teach every limitation of claim 5, Poisner cannot support a prima facie case of anticipation. The anticipation rejection is untenable and should be withdrawn. Claim 8 depends on claim 5 and further describes that the signal generating means includes means for recording the step executed according to the signal generated for recovery. This feature also is not taught in Poisner. Thus, claim 8 is patentable over Poisner based on the same reasons for claim 5 as well as on its own merits. Favorable reconsideration of claims 5 and 8 is respectfully requested.

Claim 9, as amended, describes a method of supervising a failure of a system using a plurality of timers. Several steps are performed, including (a) counting down one of the

plurality of timers if the timer is activated and not reset; (b) generating a signal for recovering if the timer goes time out, and when the signal for recovery is generated, executing a corresponding one of the steps of (i) setting a flag, (ii) outputting an interrupt signal, (iii) outputting a non-maskable interrupt and (iv) outputting a system reset signal; and (c) if the system fails to recover from the failure, repeatedly executing the steps (a) and (b) for another one of the plurality of timers. Each time the signal for recovery is generated, a corresponding one of the steps (i) to (iv) is executed in a manner that steps (i) to (iv) are executed sequentially one by one when steps (a) to (c) are repeatedly executed. In this manner, the system recovers from the failure in accordance with the degree of the failure progressively each time the step (c) is executed. Furthermore, a plurality of registers are provided and a plurality of conditions are respectively set for resetting the plurality of timers. The plurality of conditions corresponds to plural sets of values set in the plurality of registers, respectively. A reset operation to be performed on one of the plurality of registers corresponds to one of the plurality of conditions each time the step (c) is executed. Appropriate support for the amendment can be found in, for example, Figs. 1-4; page 3, line 23 though page 4, line 19; and page 10, line 2 through page 11 line 5.

Poisner, however, does not teach every limitation of claim 9. Although Poisner discusses executing a plurality of proceedings, such as interruption, reactivation, etc., in a stepwise manner, Poisner uses only one timer to perform the countdown. Thus, Poisner's system does not teach using a plurality of timers to monitor system failures. As disclosed in this case, for example, the use of plural timers provides the capacity to monitor operations of each of a plurality of processors. Poisner also fails to teach the various steps performed related to each of the plurality of timers, as described in claim 9. Furthermore, Poisner fails

to teach providing a plurality of registers for storing values to be compared with a plurality of conditions, as described in claim 9. Since Poisner fails to teach every limitation of claim 9, Poisner cannot support a prima facie case of anticipation. The anticipation rejection is untenable and should be withdrawn. Favorable reconsideration of claim 9 is respectfully requested.

New Claims 10-12 Are Patentable

By this Response, claims 10-12 are newly added. Claims 10-12 depend on independent claims 1, 5 and 9, respectively, and further describe that information is written into the plurality of registers from a supervisee, such as an operating system being monitored. Appropriate support for new claims 10-12 can be found in, for example, page 7, lines 10-12 of the written description.

As pointed out earlier, claims 1, 5 and 9, the claims on which claims 10-12 depend, are patentable over Poisner because Poisner fails to teach every limitation of claims 1, 5 and 9. Furthermore, Poisner fails teach that information is written into the plurality of registers from a supervisee, as described in claims 10-12. Therefore, claims 10-12 are patentable over Poisner by virtue of their respective dependencies on claims 1, 5 and 9, as well as based on their own merits. Favorable consideration of claims 10-12 is respectfully requested.

The Objection to the Title Is Addressed

The original title of the application was objected to for being non-descriptive. By this Response, the title is amended to "FAILURE SUPERVISING METHOD AND

APPARATUS USING PROGRESSIVE CORRECTIONS," to reflect the capacity of the method and apparatus for progressively recovering a system from failures. It is respectfully submitted that the amended title properly indicates features described in the claims.

For the reasons given above, Applicants believe that this application is conditioned for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the examiner is invited to contact Applicants' representatives listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Expires: March 1, 2005

Harry I. Moatz
Director of Enrollment and Discipline